corresponding substantially to the first layer active circuit feature and which is separated from the first layer active circuit feature by a distance. The method also includes creating a second layer of the integrated circuit having at least one circuit area, the second layer circuit area including a second active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features. The circuit and kerf areas of the first and second layers are substantially superimposed. The second layer kerf area includes a second measurement feature corresponding substantially to the second layer active circuit feature and which is separated therefrom by a distance. The distance of separation between the separated second layer active circuit feature and the second layer kerf measurement feature in the direction that the overlay error is to be determined is the same as the distance of separation between the separated first layer active circuit feature and the first layer kerf measurement feature in such direction. The second layer kerf measurement feature is displaced from the first layer kerf measurement feature compared to the first and second active circuit features in a direction perpendicular to the direction that the overlay error is to be determined. The method then includes determining a common point of reference of each of the first and second layer kerf measurement features, and measuring distance of separation in the direction of overlay error between the common points of reference of each of the first and second layer kerf measurement features to determine overlay error of the first and second active circuit features.

In another aspect, the present invention is directed to an integrated circuit wafer adapted to measure overlay error between layers made by a lithographic process. The wafer includes a first layer of the integrated circuit having at least one circuit area. The first layer circuit area includes a first active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features. The first layer kerf area includes a first measurement feature corresponding substantially to the first layer active circuit feature and which is separated from the first layer active circuit feature by a distance. The wafer also includes a second layer of the integrated circuit having at least one circuit area. The second layer circuit area includes a second active circuit feature and a kerf area adjacent to the circuit area substantially

free of active circuit features. The circuit and kerf areas of the first and second layers are substantially superimposed. The second layer kerf area includes a second measurement feature corresponding substantially to the second layer active circuit feature and separated therefrom by a distance. The distance of separation between the separated second layer active circuit feature and the second layer kerf measurement feature in the direction that the overlay error is to be determined is the same as the distance of separation between the separated first layer active circuit feature and the first layer kerf measurement feature in such direction. The second layer kerf measurement feature is displaced from the first layer kerf measurement feature compared to the first and second active circuit features in a direction perpendicular to the direction that the overlay error is to be determined. Common points of reference of each of the first and second layer kerf measurement features are determinable to permit measurement of any separation between the common points of reference of each of the first and second layer kerf measurement features to determine overlay error.

In the method and wafer of the present invention, preferably the first and second active circuit features corresponding to the first and second layer kerf measurement features are in contact with each other. The first and second layers of the integrated circuit each may have a plurality of circuit areas separated by kerf areas. Preferably, the second layer kerf measurement feature is displaced from the first layer kerf measurement feature by a distance sufficient to distinguish the corresponding active features in the circuit area so that the first and second layer kerf measurement features are more easily discerned. The common points of reference of the first and second layer kerf measurement features may comprise centerlines or edges of the features. The measurement features in the kerf areas are adapted to be destroyed when the plurality of circuit areas are cut apart.

Brief Description of the Drawings

The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The figures are for illustration purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows taken in conjunction with the accompanying drawings in which:

Fig. 1 is a top plan view of one embodiment of an active integrated circuit structure made up of components formed on two different layers with proper alignment.

Fig. 2 is a top plan view of the active integrated circuit structure of Fig. 1 with the different layer components misaligned.

Fig. 3 is a top plan view of a measurement structure corresponding substantially to the active integrated circuit structure of Fig. 1, formed in the wafer kerf area and having the different layer components displaced.

Fig. 4 is a top plan view of a measurement structure corresponding substantially to the misaligned active integrated circuit structure of Fig. 2, formed in the wafer kerf area and having the different layer components displaced.

Fig. 5 is a top plan view of a second embodiment of an active integrated circuit structure made up of components formed on two different layers with proper alignment.

Fig. 6 is a top plan view of the active integrated circuit structure of Fig. 5 with the different layer components misaligned.

Fig. 7 is a top plan view of a measurement structure corresponding substantially to the active integrated circuit structure of Fig. 5, formed in the wafer kerf area and having the different layer components displaced.

Fig. 8 is a top plan view of a measurement structure corresponding substantially to the misaligned active integrated circuit structure of Fig. 6, formed in the wafer kerf area and having the different layer components displaced.